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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,608	08/25/2003	S. Brandon Keller	100111235-1	2834

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EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,608	KELLER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04;1/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/647,608 field on 8/25/2003.

Claims 1-15 remain pending in the application.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "a cumulative value of a design element characteristic" needed to be defined as what it is. What the design element characteristic is refereed to. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being obvious over Kurosaka et al. (5,949,691).

5. As to claim 1, Kurosaka et al. teach a method and a logic circuit verification device to verify the logic circuit equivalence. Kurosaka et al. teach that the correspondence rules comprising rules to define identical name and different name, corresponding location referring to signal name and instance name, and signal/logic definition comprising signal type, logic type, particular signal and particular instance (Fig. 4-7). The hierarchical information and circuit information are as described are stored in a storage medium for retrieval and comparison. Based these above

correspondence rules, the stored circuit information could be a first list that defines a gate signal name for each instance of a first type of design elements and a second list that defines a gate signal name for each instance of a second type of the design elements. The stored information is used to comparison in order to determine unmatched design elements, thereby an orphan gate signal names that appear in only one list could be determined (col. 9-12). Kurosaka et al. do not explicitly teach storing a cumulative value of a design element characteristic for each instance of the first list and the second list and summing the cumulative value for the design characteristic corresponding to each said first type of design element gate signal name that matches one of the orphan gate signal name in order to produce a total design element characteristic value. From the above teachings, it would be obvious to one of ordinary skill in the art at the time the invention was made the claimed invention because by performing searching within the stored information as taught by Kurosaka et al. (Fig. 9A-9B), the first type of design elements gate signal name that matches one the orphan gate signal names would be easily found or unmatching information can be found, thereby a total design element characteristic value would be obtained by summing all characteristic values of design elements of the same type of the design elements.

6. As to claim 2, Kurosaka et al. teach storing circuit information as in table index (in harsh table which is known to one skill in the art) (col. 9-10). Because each of logic type inherently includes its circuit characteristic, therefore these logic types are stored in a harsh table for retrieval and comparison.

7. As to claim 3, Kurosaka et al. teach logic types, therefore the logic types would be selected from a family of well known design elements consisting of transistors, wires, capacitors, resistors and power sources.

Allowable Subject Matter

8. Claims 4-15 are allowed over the prior art of record. The prior art does not teach a first list of P-FETs, a second list of N-FETs, storing a cumulative value corresponding to a source current for each instance of the P-FETs and N-FETs, performing a set difference operation to determine orphan gate signal names and determining a cumulative value for the source current by summing all source current of each P-FETs gate signal name that matches on the orphan gate signal names in order to provide a total source current value.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER